21st International Conference on Simulation of Semiconductor Processes and Devices

Le Meridien Grand Hotel, Nuremberg, Germany
Scientific Sessions: September 6-8, 2016
Workshop Day: September 5, 2016

Conference Information and Program

Status as of August 8, 2016

SISPAD 2016

Fraunhofer IISB

IEEE Electron Devices Society

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Table of Contents

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Conference Information

Welcome to the SISPAD 2016 in Nuremberg!

The International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) provides an international forum for the presentation of leading-edge research and development results in the area of process and device simulation. SISPAD is one of the longest-running conferences devoted to technology computer-aided design (TCAD) and advanced modeling of novel semiconductor devices and nano electronic structures.

Conference Organizers

Fraunhofer Institute for Integrated Systems and
Device Technology IISB, Erlangen, Germany

Conference Chair: Dr. Jürgen Lorenz
Conference Co-Chair: Dr. Peter Pichler
Publication Chair: Dr. Eberhard Bär

Conference Office:
Barbara Progscha
Anka Wahl

www.sispad2016.org

The City of Nuremberg

The old imperial city of Nuremberg is one of the most attractive destinations for visitors from all over the world. This is due to the unique mix of history, modern age and future together with art, culture and technology of world significance.



Imperial castle, Albrecht-Dürer-Haus, and Germanisches Nationalmuseum with Way of Human Rights (© photos: Stadt Nürnberg)

www.nuernberg.de

Conference Location

The SISPAD 2016 will take place in the international conference hotel "Le Meridien Grand Hotel Nuremberg" which is located centrally opposite Nuremberg central train station and at the entrance to the historic Old Town. "Le Meridien Grand Hotel Nuremberg" is the first hotel on the square and guests can easily reach many sights on foot. In several hotels nearby, block reservations for the conference participants have been made.

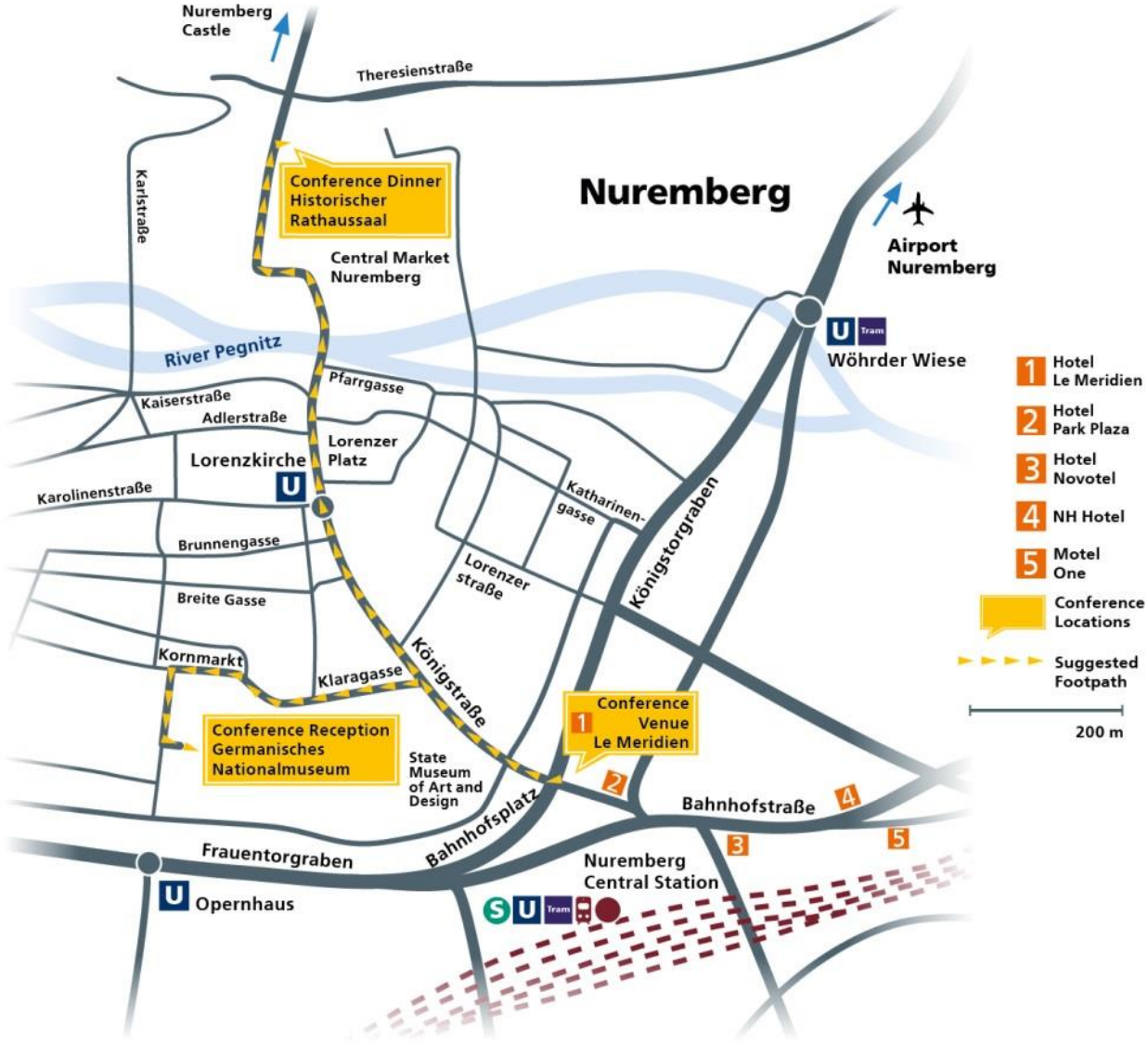
Travel Information

Air Connection
Albrecht Dürer Aiport Nuremberg is located close to the city with direct subway connection (12 min, subway line U2) to Nuremberg central train station. Furthermore, there are train connections to Nuremberg from Frankfurt airport (2.5 h) and Munich airport via Munich central station (2 h), as well as a bus shuttle service from Munich airport (2 h, reservation required).

Railway Connection
Nuremberg is a junction on the European high-speed rail network with ICE and EC / IC services at hourly intervals. Good train connections allow you to go to several other touristic sites, such as Bamberg (Unesco World Cultural Heritage), Munich, Würzburg, Regensburg (Unesco World Cultural Heritage), or Rothenburg.

Motorway Connection
Nuremberg is directly connected to the freeway. Inside the city, the traffic and parking guidance system provides direction.

In the map below you will find the conference venue (Le Meridien Grand Hotel), the hotels with the SISPAD block reservations, as well as the locations for the conference reception and the conference dinner.



Organizational Information

Conference location
Le Meridien Grand Hotel Nuremberg
Bahnhofstraße 1-3
90402 Nuremberg, Germany
Phone +49 911 2322 0

Phone numbers
During the conference, the organizers can be reached via cellular phone:
+49 176 50 26 85 49 or +49 176 54 00 85 67

Registration for the SISPAD conference

Monday, September 5	9:00 – 17:00
Tuesday, September 6	8:00 – 18:00

Wednesday, September 7	8:00 – 18:00
Thursday, September 8	8:00 – 17:00

Registration for the workshops
Please refer to the workshop information on pages 6/7.

Social events

Tuesday, September 5, 19:00 – 22:00, Germanisches Nationalmuseum (Kartäusergasse 1, 90402 Nuremberg):
Guided museum tours (different topics, see below) and conference reception

- *The Behaim Globe:* Visit one of the absolute highlights of the German National Museum, the world-famous Behaim Globe as an evidence for Nuremberg's great scientific achievements in the course of history.
- *Albrecht Dürer and his Time:* Learn about Nuremberg's famous son Albrecht Dürer and his artistic background and find out about his manifold artistic skills.
- *Medieval Architecture:* Discover the unique ensemble of architecture from the 14th century with its well-preserved cloisters, its church, the monks' dwellings and the little monastery courtyard.

Wednesday, September 6, 19:15 – 23:00, Historischer Rathaussaal (Rathausplatz 2, 90403 Nuremberg):
Conference dinner

Oral presentations
Speakers which have not submitted their presentation file before the conference can upload their presentation file (Power Point or pdf) in the lecture room before the session starts.

Posters
The poster walls will be available for mounting the posters (format A0: width=841 mm, height=1189 mm) from Wednesday (September 7) noon on. Mounting material will be provided.

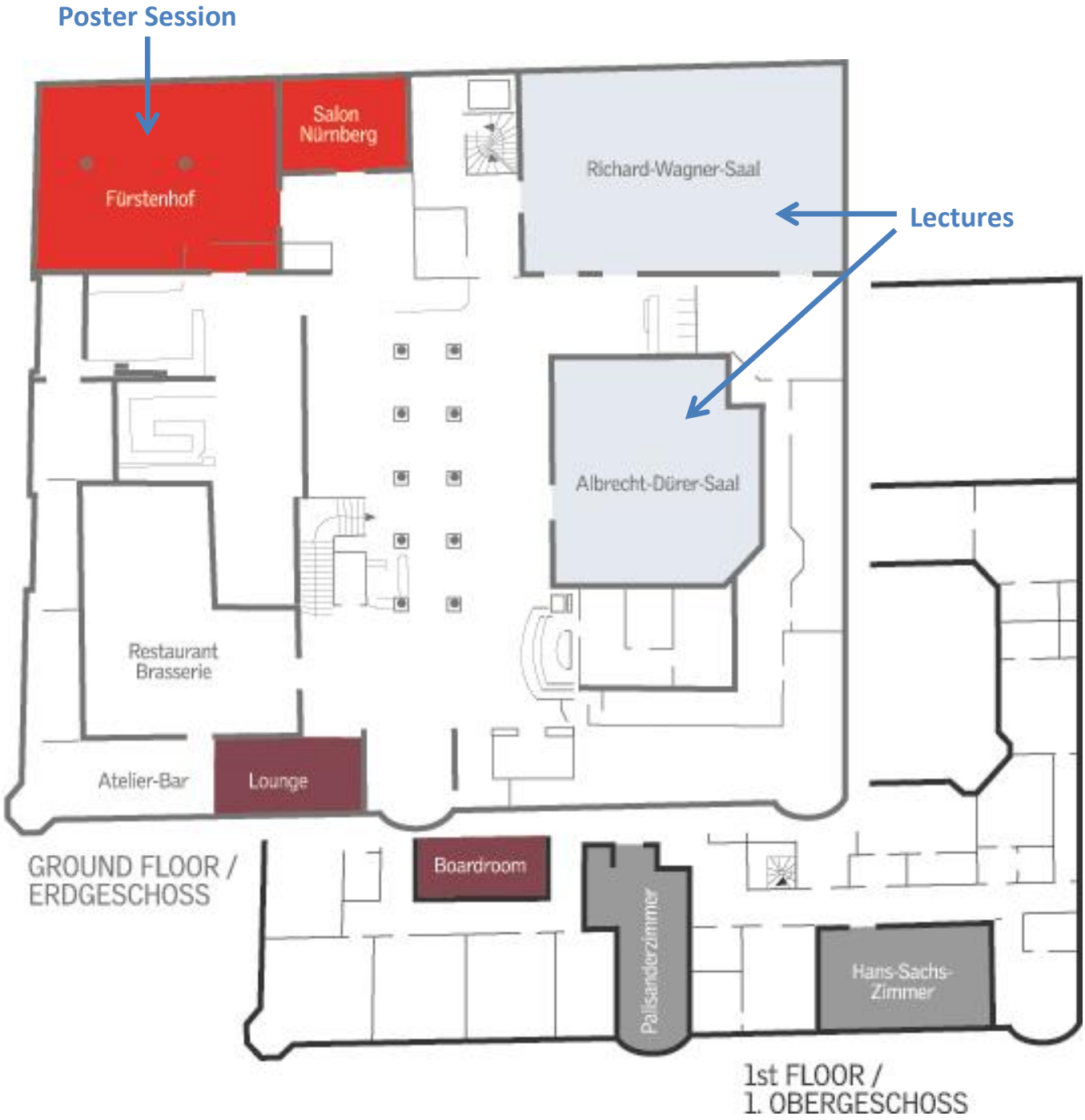
Badges
Please wear your conference badge at all times when participating in the scientific sessions and official social events.

Language
The conference language is English and will be used for all presentations and printed material.

Conference Agenda

The conference starts with a Workshop Day on Monday (September 5), followed by the official opening on Tuesday (September 6) morning and three days of conference sessions till the afternoon of Thursday (September 8).

Floor Plan of the Conference Rooms



SISPAD Workshops Monday, September 5

Workshop 1: Simulation of Advanced Interconnects
Organizers: S. Amoroso (Gold Standard Simulations), E. Baer (Fraunhofer IISB), L. Filipovic (TU Wien)

8:45	Registration	
9:00	Keynote: Status and Future of Advanced Interconnects and the Needs for Simulation	O. Faynot, CEA-LETI
9:45	Performance of Doped Carbon Nanotubes Interconnects	A. Todri-Sanial, University of Montpellier
10:30	Challenges and Simulation Solutions for Advanced Lithography for Nanometer Interconnect Patterning	P. Evanschitzky, Fraunhofer IISB
11:15	Coffee Break	
11:30	Process Simulation Models and their Application to Interconnect Manufacturing	E. Baer, Fraunhofer IISB
12:15	Thermal, Electrical, Mechanical, and Reliability Simulation for Interconnects	L. Filipovic, TU Wien
13:00	Lunch	
14:00	Tools for Simulation Workflow Management and their Application to Interconnect Modeling	S. Amoroso, Gold Standard Simulations
14:45	Physical Modeling and Numerical Optimization of the Transient Inductive Behaviour of Busbar Structures in Power Modules (Theoretical Concepts, Computational Approaches, Demonstration and Case Study)	V. Basler, G. Wachutka, TU Muenchen
16:00	Live Demonstration of Tools for Interconnect Simulation	

Workshop 2: Spin-Dependent Phenomena for New Device Applications
Organizers: V. Sverdlov, T. Grasser (Institute for Microelectronics, TU Wien)

9:00	Registration	
9:30	Ultrafast and Gigantic Spin Injection in Semiconductors	Marco Battiato (TU Wien)
10:15	New Developments in Spin Transport Phenomena in Magnetic Tunnel Junctions	Mairbek Chshiev (Univ. Grenoble Alpes and INAC CEA, Grenoble)
11:00	Coffee Break	
11:30	Logic-in-Memory	Thomas Windbacher (TU Wien)
12:15	Nanomagnetic Logic - from Micromagnetics to Circuit-Level Simulations	Markus Becherer (TU Muenchen)
13:00	Lunch	
14:00	Electrical Switching of an Antiferromagnet	Tomas Jungwirth (Academy of Sciences, Czech Republic and University of Nottingham, UK)
14:45-15:30	Silicon Quantorm Spintronics: Progress and Prospects	Rajib Rahman (Purdue University, IN USA)

Workshop 3: Variability-Aware Design Technology Co-Optimization
Organizers: A. Asenov (Glasgow University), J. Lorenz (Fraunhofer IISB)

9:00	Registration	
9:30	Welcome and Orientation	J. Lorenz (Fraunhofer IISB)
9:45	Challenges and Prospects for Variability-Aware DTCO	A. Asenov (Glasgow University)
	Session on Related European Projects (EP)	
10:00	EP 1: Outline and Selected Results of the EC FP7 Project SUPERTHEME	J. Lorenz (Fraunhofer IISB)
10:30	EP 2: Physical Models for Variation-Aware Device Simulation	M. Nedjalkov (TU Wien)
11:00	Coffee Break	
	Session on Related European Projects (cont.)	
11:30	EP 3: Variability-Aware Compact Models	C. Millar (GSS)
12:00	EP 4: Modeling of Variability under Reliability: The MORV Project	D. Helms (OFFIS)
12:30	EP 5: Variability from Equipment to Circuit: The Horizon2020 Project SUPERAID7	J. Lorenz (Fraunhofer IISB)
13:00	Lunch	
14:00	Variation Source Identification and Control with Behavioral Modeling	W. Clark (Coventor)
14:30	Pathfinding through DTCO: PPA Evaluation of 5 nm Technology	P. Asenov / V. Moroz (Synopsys)
15:00	Talk on the Industrial Perspective	to be confirmed
15:30	Panel Discussion on Challenges and Solutions of Variation-Aware DTCO	

Overview of Scientific Sessions

Tuesday, September 6	
	Plenary Session A
9:00- 9:15	Jürgen Lorenz (Fraunhofer IISB): **Welcome**
9:15-10:00	Mark Law (University of Florida): **20 Years of SISPAD: Adolescence of TCAD and Further Perspectives (Keynote)**
10:00-10:40	Andre Juge (STMicroelectronics): **Device Level Modeling Challenges for Circuit Design Methodology in Presence of Variability (invited)**
10:40-11:10	Coffee break
11:10-12:30	Parallel Sessions **1: Nanowires** **2: Process Simulation at Various Levels**
12:30-14:00	Lunch
	Plenary Session B
14:00-14:40	Yoshinari Kamakura (Osaka Univ.): **Full Band Monte-Carlo Simulation of Impact Ionization in Wide Bandgap Semiconductors Based on Ab Initio Calculation (invited)**
14:40-15:40	Parallel Sessions **3: III/V Device Simulation** **4: Boltzmann Transport I**
15:40-16:20	Coffee break
16:20-17:40	Parallel Sessions **5: TunnelFETs** **6: Atomistic Simulation**
19:00-22:00	**Guided Museum Tours and Conference Reception at "Germanisches Nationalmuseum"**

Wednesday, September 7	
	Plenary Session C
9:00-9:40	Seonghoon Jin (Samsung): **Performance Evaluation of FinFETs: From Multisubband BTE to DD Calibration (invited)**
9:40-10:40	Parallel Sessions **7: Power Device Simulation I** **8: Equipment-Related Process Simulation**
10:40-11:10	Coffee Break
11:10-12:30	Parallel Sessions **9: Emerging Memory Devices I: Resistive Switching** **10: Compact Modeling**
12:30-14:00	Lunch
	Plenary Session D
14:00-14:40	Suman Datta (Univ. Notre Dame): **In Quest of the Next Switch (invited)**
14:40-15:20	Parallel Sessions **11: Power Device Simulation II: IGBT** **12: Boltzmann Transport II**
15:40-17:40	**Poster Session**
19:15-23:00	**Conference Dinner at "Historischer Rathaussaal"**

Thursday, September 8	
9:00-9:40	Plenary Session E Mathieu Luisier (ETH Zurich): **Atomistic Simulation of Nanodevices (invited)**
9:40-10:40	Parallel sessions **13: FinFET & Trigate** **14: Variations**
10:40-11:10	Coffee Break
11:10-12:10	Parallel Sessions **15: Emerging Memory Devices II** **16: High Frequency/Noise**
12:10-13:40	Lunch
13:40-14:20	Plenary Session F Terry Ma (Synopsys): **Future Perspectives of TCAD in Industry (invited)**
14:20-15:00	Parallel sessions **17: SiGe Device Simulation** **18: Monte-Carlo Simulation**
15:00-15:40	Coffee break
15:40-16:40	Parallel Sessions **19: Graphene** **20: DFT and NEGF**
16:40	**Close of conference**

Scientific Sessions in Detail

Tuesday, September 6		
9:00	**Plenary Session A (Richard-Wagner-Saal) Chair: J. Lorenz (Fraunhofer IISB)**	
9:00	**Welcome** J. Lorenz (Fraunhofer IISB)	
9:15	**Keynote I1: 20 Years of SISPAD: Adolescence of TCAD and Further Perspectives** M. Law (University of Florida)	
10:00	**Invited I2: Device Level Modeling Challenges for Circuit Design Methodology in Presence of Variability** A. Juge (STMicroelectronics)	
10:40	**Coffee break**	
11:10	**Session 1: Nanowires (Richard-Wagner-Saal)** **Chairs: D. Esseni (Univ. Udine),** **Y. Kamakura (Osaka Univ.)**	**Session 2: Process Simulation at Various Levels (Albrecht-Dürer-Saal)** **Chairs: P. Oldiges (IBM), D. Tsoukalas (NTUA Athens)**
11:10	**O1.1: Numerical Investigation of Junctionless Silicon Nanowire Transistors by a Deterministic Boltzmann/Schrödinger/Poisson Solver** M. Noei, C. Jungemann (Chair of Electromagnetic Theory, RWTH Aachen)	**O2.1: Atomistic Predictions of Substrate Orientation Impact during SiGe Alloys Solid Phase Epitaxial Regrowth** A. Payet_†‡§, B. Sklénard†‡, J.-C. Barbé†‡, P. Batude†‡, R. Gonella*, P. Gergaud†‡, I. Martin-Bragado§¶ (*STMicroelectronics; †Univ. Grenoble Alpes; ‡CEA,LETI; §IMDEA Materials Institute; ¶Synopsys Inc.)
11:30	**O1.2: Modeling the Thermal Conductivity of Si Nanowires with Surface Roughness** K. Vuttivorakulchai, M. Luisier, A. Schenk (ETH Zurich)	**O2.2: Atomistic Study of the Anisotropic Elastic Interaction between Extended and Point Defects in Crystalline Silicon and Its Influence on Si Self-interstitial Diffusion** I. Santos[1], M. Aboy[1], L.A. Marques1, A.M. Hernández-Díaz[2], P. Castrillo[2], P. López[1], M. Ruiz[1], L. Pelaz[1] ([1]Universidad de Valladolid, Spain, [2]UCAM, Universidad Católica de Murcia, Spain)
11:50	**O1.3: One-Dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nanowire Transistors** T. Sadi[1], E. Towie[2], M. Nedjalkov[3], C. Riddet[2], C. Alexander[2], L. Wang[1,2], V. Georgiev[1], A. Brown[2], C. Millar[2], A. Asenov [1,2] ([1]University of Glasgow; [2]Gold Standard Simulations Ltd, [3]Institute for Microelectronics, TU Wien)	**O2.3: Empirical Cluster Modeling Revisited** P. Pichler (Fraunhofer Institute for Integrated Systems and Device Technology IISB and Chair of Electron Devices, University of Erlangen-Nuremberg)
12:10	**O1.4: Band-to-Band Tunneling Off-State Leakage in Ge Fins and Nanowires: Effect of Quantum Confinement** G. Eneman, A.S. Verhulst, L. Smith[1], V. Moroz[1], A. De Keersgieter, A. Mocuta, N. Collaert, A. Thean (Imec, [1]Synopsys)	**O2.4: A Million Wafer, Virtual Fabrication Approach to Determine Process Capability Requirements for an Industry-Standard N5 BEOL Two-Level Metal Flow** W. F. Clark[1], C. J. Wilson[2], G. Pourtois[2], M. Gallagher[2], A. De Jamblinne[2], D. Piumi[2], J. Boemmels[2], Z. S. Tokei[2], D. Mocuta[2], A. Juncker[1], E. Paladugu[3], D. Fried[3] ([1]Coventor SARL,; [2]imec; [3]Coventor Inc.)
12:30-14:00	**Lunch**	

Tuesday, September 6, continued		
	Plenary Session B (Richard-Wagner-Saal) Chair: M. Rudan (ARCES – Univ. Bologna)	
14:00	**Invited I3: Full Band Monte-Carlo Simulation of Impact Ionization in Wide Bandgap Semiconductors Based on Ab-Initio Calculation** Y. Kamakura (Osaka Univ.)	
	Session 3: III/V Device Simulation (Richard-Wagner-Saal) Chair: M. Rudan (ARCES – Univ. Bologna)	**Session 4: Boltzmann Transport I (Albrecht-Dürer-Saal) Chair: S. Jin (Samsung)**
14:40	**O3.1: Drift-Diffusion Quantum Corrections for $In_{0.53}Ga_{0.47}As$ Double Gate Ultra-Thin-Body FETs** P. Aguirre, H. Carrillo-Nuñez, A. Ziegler, M. Luisier, A. Schenk (ETH Zurich)	**O4.1: Phase-Space Solution of the Subband Boltzmann Transport Equation for Nano-Scale TCAD** Z. Stanojević, M. Karner, O. Baumgartner, HW. Karner, C. Kernstock, H. Demel, F. Mitterbauer (Global TCAD Solutions GmbH)
15:00	**O3.2: Examination of the InP/InGaAs Single-Photon Avalanche Diodes by Establishing a New TCAD-Based Simulation Environment** T. Knežević*, T. Suligoj (University of Zagreb)	**O4.2: Hydrodynamic Electron Transport and Terahertz Plasma-Wave Oscillation in Topological Insulator FETs (TI-FETs)** Z. Denga, J. Jiangb, S. Donga, L. Zhanga, J. Zhanga, Y. Wanga, Z. Yua (Tsinghua University)
15:20	**O3.3: Simulation of AlGaN/GaN Rake-Gate HFET: A Novel Normally-Off HFET Based on Stress and Layout Engineering** H. Y. Wong, N. Braga, R. V. Mickevicius (Synopsys, Inc.)	**O4.3: Modeling Topological-Insulator Field-Effect Transistors Using the Boltzmann Equation** W.G. Vandenberghe, M.V. Fischetti (University of Texas at Dallas)
15:40	**Coffee break**	
	Session 5: TunnelFETs (Richard-Wagner-Saal) Chairs: C. Jungemann (RWTH Aachen), A. Burenkov (Fraunhofer IISB)	**Session 6: Atomistic Simulation (Albrecht-Dürer-Saal) Chairs: S. Datta (Univ. Notre Dame), M. Luisier (ETH Zurich)**
16:20	**O5.1: Transfer Matrix Based Semiclassical Model for Field-Induced and Geometrical Quantum Confinement in Tunnel FETs** S. Sant, H. Carrillo-Nuñez, M. Luisier, A. Schenk (ETH Zurich)	**O6.1: Orbitronics - Harnessing Metal Insulator Phase Transition in 1T-$MoSe_2$** R. K. Ghosh, S. Datta (University of Notre Dame)
16:40	**O5.2: Efficient TB-NEGF Simulations of Ultra-Thin Body Tunnel FETs** W. J. Jeong, J. Seo, M. Shin (Korea Advanced Institute of Science and Technology)	**O6.2: Atomistic Simulation of Transport Properties of Non-Graphitic Armchair Nanotubes and Effect of Stone-Wales Defects** A. Sengupta (Indian Institute of Engineering Science and Technology)
17:00	**O5.3: A Possible Explanation of the Record Electrical Performance of Silicon Nanowire Tunnel FETs with Silicided Source Contacts** A. Burenkov, J. Lorenz (Fraunhofer Institute for Integrated Systems and Device Technology IISB)	**O6.3: Atomistic Simulation Flow for Source-Drain Epitaxy and Contact Formation Processes of Advanced Logic Devices** S.-Y. Lee[a], A. Schmidt[a], I. Jang[a], D. S. Kim[a], R. Chen[b], C. Ahn[b], W. Choi[b], K.-H Lee[a] ([a]Samsung Electronics Co Ltd, [b]Samsung Semiconductor Inc.)
17:20	**O5.4: Full-Band Simulations of Resonant Tunneling in Transition Metal Dichalcogenide-Based Interlayer Tunnel Field-Effect Transistors** X. Wu, X. Mou, L. F. Register, S. K. Banerjee (University of Texas at Austin)	**O6.4: Grain Boundary Resistance in Nanoscale Copper Interconnections** D. Valencia[1], E. Wilson[1], Z. Jiang[1,2] , P. Sarangapani[1], G. Klimeck[1], M. Povolotskyi[1] ([1] Purdue University, [2]Samsung Semiconductor Inc.)
19:00-22:00	**Guided Museum Tours and Conference Reception at "Germanisches Nationalmuseum"**	

Wednesday, September 7		
	Plenary Session C (Richard-Wagner-Saal) Chair: M. Law (Univ. of Florida)	
9:00	**Invited I4: Performance Evaluation of FinFETs: From Multi-Subband BTE to DD Calibration** S. Jin (Samsung)	
	Session 7: Power Device Simulation I (Richard-Wagner-Saal) **Chair: M. Law (Univ. of Florida)**	**Session 8: Equipment-Related Process Simulation (Albrecht-Dürer-Saal)** **Chair: C. Millar (Gold Standard Simulations)**
9:40	**O7.1: Comparative Study of Contact Topographies of 4.5kV SiC MPS Diodes for Optimizing the Forward Characteristics** Y. Huang, G. Wachutka (Technical University of Munich)	**O8.1: 3D Simulation of Light Exposure and Resist Effects in Laser Direct Write Lithography** T. Onanuga[1,2], A. Erdmann[1,2] ([1]Fraunhofer Institute for Integrated Systems and Device Technology IISB; [2]Friedrich-Alexander-Universität Erlangen-Nürnberg)
10:00	**O7.2: A Simulation Model for SiC Power MOSFET Based on Surface Potential** Y. Nakamura†, M. Shintani††, K. Oishi††, T. Sato††, T. Hikihara† (†Graduate School of Engineering ††Graduate School of Informatics, Kyoto University)	**O8.2: Automated Source/Mask/Directed Self-Assembly Optimization Using a Self-Adaptive Hierarchical Modeling Approach** T. Fühner[a], P. Michalak[a], X. Wu[a,b], A. Erdmann[a] ([a]Fraunhofer Institute for Integrated Systems and Device Technology IISB; [b]University of Hong Kong)
10:20	**O7.3: 3D TCAD Analysis of the Effect on dI/dt of Cathode Shorts in Phase Controlled Thyristors** M. Bellini, J. Vobecký (ABB Switzerland Ltd)	**O8.3: Equipment Simulation for Studying the Growth Rate and its Uniformity of Oxide Layers Deposited by Plasma-Enhanced Oxidation** E. Baer [1], Juergen Niess [2] ([1] Fraunhofer Institute for Integrated Systems and Device Technology IISB; [2] HQ-Dielectrics GmbH)
10:40	**Coffee break**	
	Session 9: Emerging Memory Devices I: Resistive Switching (Richard-Wagner-Saal) **Chairs: A. Schenk (ETH Zurich), V. Degtyarov (INTEL)**	**Session 10: Compact Modeling (Albrecht-Dürer-Saal)** **Chairs: P. Chang (TSMC), A. Juge (ST)**
11:10	**O9.1: KMC Simulation of the Electroforming, Set and Reset Processes in Redox-Based Resistive Switching Devices** E. Abbaspour[a], S. Menzel[b], C. Jungemann[a] ([a]Institute of Electromagnetic Theory, RWTH Aachen; [b]Forschungszentrum Jülich)	**O10.1: TCAD Proven Compact Modelling Re-Centring Technology for Early 0.x PDKs** L. Wang[a], b, B. Cheng[b], P. Asenov[b], A. Pender[b], D. Reid[b], F. Adamu-Lema[a], C. Millar[b], A. Asenov[a,b] ([a] University of Glasgow; [b] Gold Standard Simulations Ltd)
11:30	**O9.2: A 2D Axisymmetric Dynamic Drift-Diffusion Model for Numerical Simulation of Resistive Switching Phenomena in Metal Oxides** A. Marchewka[a], R. Waser[a,b], S. Menzel[b] ([a] Institut für Werkstoffe der Elektrotechnik II, RWTH Aachen University; [b] Forschungszentrum Jülich)	**O10.2: Thermal Effect and Compact Model in Three-Dimensional (3D) RRAM Arrays** N. D. Lu, Z. W. Zong, P. X. Sun, L. Li, Q. Liu, H. B. Lv, S. B. Long, M. Liu (Key Laboratory of Microelectronic Devices & Integrated Technology, IMECAS)
11:50	**O9.3: Advanced Physical Modeling of SiO_x Resistive Random Access Memories** T. Sadi[1], L. Wang[1,2], D. Gao[3], A. Mehonic[4], L. Montesi[4], M. Buckwell[4], A. Kenyon[4], A. Shluger[3], A. Asenov[1,2] ([1]University of Glasgow; [2]Gold Standard Simulations Ltd; [3]Dept. of Physics and Astronomy, University College London (UCL); [4]Dept. of Electronic and Electrical Engineering, UCL)	**O10.3: Reconfigurable FET SPICE Model for Design Evaluation** S. Martinie, J. Lacord, O. Rozeau, C. Navarro, S. Barraud, J.-C. Barbe (CEA-LETI)
12:10	**O9.4: Atomic Monte-Carlo Simulation for CBRAM with Various Filament Geometries** Y. D. Zhao, P. Huang, Z. H. Guo, Z. Y. Lun, X. Y. Liu, J. F. Kang (Peking University)	**O10.4: Verilog-A Compact Model for a Novel $Cu/SiO_2/W$ Quantum Memristor** S. R. Nandakumar. B. Rajendran (New Jersey Institute of Technology)

12:30-14:00	**Lunch**	
Wednesday, September 7, continued		
	Plenary Session D (Richard-Wagner-Saal) Chair: K. Sonoda (Renesas)	
14:00	**Invited I5: In Quest of the Next Switch** S. Datta (Univ. Notre Dame)	
	Session 11: Power Device Simulation II: IGBT (Richard-Wagner-Saal) **Chair: K. Sonoda (Renesas)**	**Session 12: Boltzmann Transport II (Albrecht-Dürer-Saal)** **Chair: T. Grasser (TU Wien)**
14:40	**O11.1: Influence of Quasi-3D Filament Geometry on the Latch-Up Threshold of High-Voltage Trench-IGBTs** C. Toechterle[1)], F. Pfirsch[2)] , C. Sandow[2)], G. Wachutka[1)] ([1)]Institute for Physics of Electrotechnology, Technical University of Munich; [2)]Infineon Technologies AG)	**O12.1: On The Efficient Methods to Solve Multi-Subband BTE in 1D Gas Systems: Decoupling Approximations Versus the Accurate Approach** A. -T. Pham*, Z. Jiang*, S. Jin*, J. Wang*, W. Choi*, M. A. Pourghaderi†, K. -H. Lee† (*Samsung Semiconductor, Inc.; †Semiconductor R&D Center, Samsung Electronics)
15:00	**O11.2: Accurate IGBT Modeling under High-Injection Condition** A. Tone, Y. Miyaoku, M. Miura-Mattausch, U. Feldmann, H. Kikuchihara, *D. Navarro, H. J. Mattausch (Hiroshima University; *Silvaco Japan)	**O12.2: Investigation of Scattering Mechanism in Nano-Scale Double Gate $In_{0.53}$ $Ga_{0.47}As$ nMOSFETs by a Deterministic BTE Solver** S. Di[1], Z. Lun[1], P. Chang[1], L. Shen[1], K. Zhao[1,3], T. Lu[2], G. Du[1], X. Liu[1] ([1]Institute of Microelectronics, Peking University; [2]CAPT, HEDPS, IFSA Collaborative Innovation Center of MoE, LMAM & School of Mathema-tical Sciences, Peking University; [3]School of Information and Commu-nication, Beijing Information Science and Technology University)
15:20	**O11.3: Automated Vertical Design Co-Optimization of a 1200V IGBT and Diode** M. Bina, A. Philippou, M. Hauf, Ch. Sandow, F.-J. Niedernostheide (Infineon Technologies AG)	**O12.3: Deterministic Boltzmann Equation Solver for Graphene Sheets Including Self-Heating Effects** S.-M. Hong, S. Cha (Gwangju Institute of Science and Technology)
15:40-17:40	**Poster Session (Raum Fürstenhof), see page 14**	
19:15-23:00	**Conference Dinner at "Historischer Rathaussaal"** **Dinner Speech: S. Selberherr (TU Wien)**	

Thursday, September 8		
	Plenary Session E (Richard-Wagner-Saal) Chair: T. Ma (Synopsys)	
9:00	**Invited I6: Atomistic Simulation of Nanodevices** M. Luisier (Integrated Systems Laboratory, ETH Zurich)	
9:40	**Session 13: FinFET & Trigate (Richard-Wagner-Saal)** **Chair: T. Ma (Synopsys)**	**Session 14: Variations (Albrecht-Dürer-Saal)** **Chair: J.-C. Barbe (CEA/Leti)**
9:40	**O13.1: Accurate Prediction of Device Performance in Sub-10nm WFIN FinFETs Using Scalpel SSRM-Based Calibration of Process Simulations** P. Eyben , P. Matagne, T. Chiarella, A. De Keersgieter, S. Kubicek, J. Mitard, A. Mocuta, N. Horiguchi, A.V-Y. Thean (imec)	**O14.1: Simulation of Process Variations in FinFET Transistor Patterning** E. Baer, A. Burenkov, P. Evanschitzky, J. Lorenz (Fraunhofer Institute for Integrated Systems and Device Technology IISB)
10:00	**O13.2: High and Low-Field Contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework** L. Bourdet[1,2], Jing Li[1,2], J. Pelloux-Prayer[2,3], F. Triozon[2,3], M. Cassé[2,3], S. Barraud[2,3], S. Martinie[2,3], D. Rideau[4], Y.-M. Niquet[1,2] ([1] CEA, INAC-MEM, L_Sim; [2] Université Grenoble Alpes; [3] CEA, Leti; [4] STMicroelectronics)	**O14.2: Process Informed Accurate Compact Modelling of 14 nm FinFET Variability and Application to Statistical 6T-SRAM Simulations** X. Wang[1,2], D. Reid[2], L. Wang[1,2], C. Millar[2], A. Burenkov[3], P. Evanschitzky[3], E. Baer[3], J. Lorenz[3], A. Asenov[1,2] ([1]University of Glasgow; [2]Gold Standard Simulations Ltd.; [3] Fraunhofer Institute for Integrated Systems and Device Technology IISB)
10:20	**O13.3: Charge-Collection Modeling for SER Simulation in FinFETs** U. Monga[1], J. Choi[1], J. Jeon[1], S. Choo[2], T. Uemura[2], S. Lee[2], U. Kwon[1], S. Pae[2], K.-H. Lee[1] ([1]CAE, Semiconductor R&D Centre; [2]TQR, Samsung Electronics Co., Ltd.)	**O14.3: A Comprehensive Solution for BEOL Variation Characterization and Modeling** K. Chiang, J.-F. Huang, C. Hsiao, J. Sun, C. Cheng, K.-P. Lu, K.-W. Su, C.-K. Lin, K. Chen, T.-Y. Cheng, K.-H. Tam, T.-Y. Liu, K.-Y. Su, M.-C. Jeng (Taiwan Semiconductor Manufacturing Company)
10:40	**Coffee break**	
	Session 15: Emerging Memory Devices II (Richard-Wagner-Saal) **Chair: G. Wachutka (TU München)**	**Session 16: High Frequency/Noise (Albrecht-Dürer-Saal)** **Chair: F. Register (Univ. of Texas at Austin)**
11:10	**O15.1: Physical Modeling of Ferroelectric Field-Effect Transistors in the Negative Capacitance Regime** P. Lenarczyk, M. Luisier (Integrated Systems Laboratory, ETH Zürich)	**O16.1: Electric Response of Ovonic Materials to Oscillating Potentials** E. Piccinini, R. Brunetti[1], M. Rudan, C. Jacoboni[1] (DEI Department, University of Bologna; [1]FIM Department, University of Modena and Reggio Emilia)
11:30	**O15.2: Magnetic Field Dependent Tunneling Magnetoresistance through a Quantum Well between Ferromagnetic Contacts** V. Sverdlov, .A. Makarov, T. Windbacher, S. Selberherr (Institute for Microelectronics, TU Wien)	**O16.2: Physical-Based RTN Modeling of Ring Oscillators in 40-nm SiON and 28-nm HKMG by Bimodal Defect-Centric Behaviors** A. Oshima, T. Komawaki, K. Kobayashi, R. Kishida*, P. Weckx§†, B. Kaczer†, T. Matsumoto‡, H. Onodera†† (* Kyoto Institute of Technology; § KU Leuven; †imec; ‡University of Tokyo; ††Kyoto University)
11:50	**O15.3: Simulation of Threshold Switching Based on an Electric Field Induced Thermal Runaway** C. Funck[a], S. Hoffmann-Eifert[b], R. Waser[a,b,] S. Menzel[b] ([a]Institut für Werkstoffe der Elektrotechnik II, RWTH Aachen University; [b]Peter Grünberg Institut, Forschungszentrum Jülich)	**O16.3: Noise Simulation of Bipolar Organic Semiconductor Devices Based on the Master Equation** W. Zhou, C. Zimmermann, C. Jungemann (Chair of Electromagnetic Theory, RWTH Aachen University)
12:10-13:40	**Lunch**	

Thursday, September 8, continued		
	Plenary Session F (Richard-Wagner-Saal) Chair: S. Selberherr (TU Wien)	
13:40	**Invited I7: Future Perspectives of TCAD in Industry** T. Ma (Synopsys)	
	Session 17: SiGe Device Simulation (Richard-Wagner-Saal) **Chair: S. Selberherr (TU Wien)**	**Session 18: Monte-Carlo Simulation (Albrecht-Dürer-Saal)** **Chair: D. Rideau (ST)**
14:20	**O17.1: Physics-Based Hot-Carrier Degradation Model for SiGe HBTs** H. Kamrani[a], D. Jabs[a], V. d'Alessandro[b], N. Rinaldi[b], C. Jungemann[a] ([a] Chair of Electromagnetic Theory, RWTH Aachen University; [b]Dept. of Electrical Eng. and Information Tech., University Federico II, Naples)	**O18.1: Advanced Quasi Self-Consistent Monte Carlo Simulations of Electrical and Thermal Properties of Nanometer-Scale Gallium Nitride HEMTs Considering Local Phonon Number Distribution** N. Ito, T. Misawa, Y. Awano (Keio University)
14:40	**O17.2: Impact of BTBT, Stress and Interface Charge On Optimum Ge in SiGe pMOS for Low Power Applications** S. Dhar[1], H.K. Noh[1], S.J. Kim[1], H.W. Kim[1], Z. Wu[1], W.S. Lee[1], A.T. Pham[2], S.H. Jin[2], K.K. Bhuwalka[1], J.C. Kim[1], C.W. Jeong[1], U.-H. Kwon[1], W.S. Choi[2], S. Maeda[3], K.-H. Lee[1] ([1]CAE, [3]LogicTD, Semiconductor R&D Center, Samsung Electronics; [2]Samsung Semiconductor Inc.)	**O18.2: Theoretical Study of Electron Transport in Silicene Using Full-Band Monte Carlo Simulations** G. Gaddemane, W. G. Vandenberghe, M. V. Fischetti (University of Texas at Dallas)
15:00	**Coffee break**	
	Session 19: Graphene (Richard-Wagner-Saal) **Chair: E. Baer (Fraunhofer IISB)**	**Session 20: DFT and NEGF (Albrecht-Dürer-Saal)** **Chair: P. Pichler (Fraunhofer IISB)**
15:40	**O19.1: Modeling Electrostatic Doping and Series Resistance in Graphene-FETs** S. Venica, M. Zanato, F. Driussi, P. Palestri, L. Selmi (University of Udine)	**O20.1: Carrier Scattering by Workfunction and Band Offset Fluctuations in High-κ/Metal Gate Stacks** Z. Zeng[1,2], F. Triozon[3,2], Y.-M. Niquet[1,2] ([1]CEA, INAC-MEM, L Sim; [2] University Grenoble Alpes; [3]CEA,INAC-MEM)
16:00	**O19.2: Models for Plasmonic THz Detectors Based on Graphene Split-Gate FETs with Lateral p-n Junctions** M. Ryzhii*, V. Ryzhii†, A. Satou†, T. Otsuji†, V. Mitin‡, M. S. Shur[§] (*University of Aizu; †Tohoku University; ‡University at Buffalo, [§]Rensselaer Polytechnic Institute)	**O20.2: Metal-InGaAs Contact Resistance Calculations from First Principles** T. Markussen, Kurt Stokbro (QuantumWise A/S)
16:20	**O19.3: Effect of Rotational Misalignment on Interlayer Coupling in a Graphene/hBN/Graphene van der Waal's Heterostructure** A. Valsaraj, L. F. Register, S. K. Banerjee (University of Texas at Austin)	**O20.3: Semiconductor Band Alignment from First Principles: a New NEGF Method Applied to the CZTSe/CdS Interface for Photovoltaics** M. L. N. Palsgaard[a/b], A. Crovetto[a], T. Gunst[a], T. Markussen[b], O. Hansen[a], K. Stokbro[b], M. Brandbyge[a] ([a]DTU Technical University of Denmark, [b]QuantumWise A/S)
16:40	**Close of conference**	

Poster Session (Wednesday, September 7, 15:40 - 17:40, Raum Fürstenhof)

P1 A New Microscopic Formalism for the Electron Scattering by Remote "Paired" Dipoles in HKMG MOSFETs
S.-H. Hsieh, J.-C. Hung, M.-J. Chen (National Chiao-Tung University)

P2 Simulation of a Graphene FET with a Deterministic Approach
O. Dieball, Z. Kargar, D. Ruic, C. Jungemann (Chair of Electromagnetic Theory, RWTH Aachen University)

P3 Compact Modeling of Power Devices Embedded in Advance Low-Power CMOS Circuits
Y. Hirano, *A. Itoh, H. Kikuchihara, T. Iizuka, M. Miura-Mattausch, H. J. Mattausch (Hiroshima University; *Broadcom)

P4 Impact of Strain on the Performance of Si Nanowires Transistors at the Scaling Limit: A Full-Band 3D Monte Carlo/2D Poisson Schrödinger Simulation Study
T. Al-Ameri[a], V. P. Georgiev[a], F.-A. Lema[a], T. Sadi[a], X. Wang[a], E. Towie[b], C. Riddet[b], C. Alexander, A. Asenov[a,b] ([a] University of Glasgow, [b]Gold Standard Simulations Ltd)

P5 First Principles Based NEGF Simulations of Si Nanowire FETs
M. Shin, W. J. Jeong, J. Lee, J. Seo (Korea Advanced Institute of Science and Technology)

P6 NEMO5: Predicting MoS_2 Heterojunctions
K.-C. Wang*, D. Valencia, J. Charles, Y. He, M. Povolotskyi, G. Klimeck, J. Maassen, M. Lundstrom, T. Kubis (Purdue University)

P7 Unified Regional Fermi-Potential-Based Compact Model for Double Heterostructure HEMTs
A. Ajaykumar, X. Zhou, B. Syamal, S. B. Chiah (Nanyang Technological University)

P8 3D MC Simulations of Strain, Channel Orientation, and Quantum Confinement Effects in Nanoscale Si SOI FinFETs
M. A. Elmessary[1,2], D. Nagy[1], M. Aldegunde[3], A. J. García-Loureiro[4], K. Kalna[1] ([1]Swansea University; [2]Mansoura University; [3]School of Engineering; [4]Universidade de Santiago de Compostela)

P9 Three-Dimensional Growth Rate Modeling and Simulation of Silicon Carbide Thermal Oxidation
Vito Šimonka*, A. Hössinger‡, J. Weinbub*, S. Selberherr† (*Christian Doppler Laboratory for High Performance TCAD at the †Institute for Microelectronics, TU Wien; ‡Silvaco Europe Ltd.)

P10 Simulation of Silicon-Dot-Based Single-Electron Memory Devices
F. J. Klüpfel, A. Burenkov, J. Lorenz (Fraunhofer Institute for Integrated Systems and Device Technology IISB)

P11 Impact of Cross-Section of 10.4 nm Gate Length $In_{0.53}Ga_{0.47}As$ FinFETs on Metal Grain Variability
N. Seoane, G. Indalecio, A.J. García-Loureiro, K. Kalna* (University of Santiago de Compostela; *Swansea University)

P12 Optimization of Reconfigurable Si NW FETs for Analog High Frequency Applications
G. Darbandy[a,b], M. Schröter[a,c], M. Claus[a,b] ([a] Chair for Electron Devices and Integrated Circuits, TU Dresden; [b] Center for Advancing Electronics Dresden (Cfaed), Technische Universtät Dresden; Department of Electrical and Computer Engineering, UC San Diego)

P13 Physical Modelling of the SET/RESET Characteristics and Analog Properties of $TiO_x/HfO_{2-x}/TiO_x$-Based RRAM Devices
P. Bousoulas, P. Asenov, D. Tsoukalas (National Technical University of Athens)

P14 Multi-Subband Ensemble Monte Carlo Study of Band-to-Band Tunneling in Silicon-Based TFETs
C. Medina-Bailon, C. Sampedro, J.L. Padilla, F. Gamiz, A. Godoy, L. Donetti (Universidad de Granada)

P15 A Simple Model for the Size-Dependent Carrier Mobilities in Gate-All-Around Silicon Devices
Z. Zeng[1,2], Y.-M. Niquet[1,2]; F. Triozon[3,2], S. Barraud[3,2] ([1]CEA, INAC-MEM, L Sim; [2]University Grenoble Alpes; [3]CEA, LETI-MINATEC)

P16 Investigation of Carbon Nanotube Based Field-Effect Transistors Using Atomistic Quantum Transport and Numerical Device Simulation
F. Fuchs[1,2,3], A. Zienert[4], J. Schuster[3], S. Mothes[2,5], M. Claus[2,5], S. Gemming[1] ([1]Helmholtz-Zentrum Dresden-Rossendorf; [2]Center for Advancing Electronics Dresden; [3]Fraunhofer Institute for Electronic Nano Systems; [4]Center for Microtechnologies, TU Chemnitz; [5]Chair for Electron Device and Integrated Circuits, TU Dresden)

P17 Using One-Dimensional Radiosity to Model Neutral Flux in Convex High Aspect Ratio Structures
P. Manstetten*, L. Filipovic†, A. Hössinger‡, J. Weinbub*, S. Selberherr† (*Christian Doppler Laboratory for High Performance TCAD at the †Institute for Microelectronics, TU Wien; ‡Silvaco Europe Ltd.)

P18 Deterministic Solutions of the Boltzmann Equation for Charge Transport in Graphene on Substrates
A. Majorana, G. Mascali, V. Romano (University of Catania)

P19 Performance Analysis of p-Type Silicon Nanowire FETs with Silicon-Germanium Cladding
M. Frey*, J. Huang‡, F. Heinz*, A. Erlebach*, L. Smith‡, V. Moroz‡ (*Synopsys Switzerland LLC; ‡Synopsys, Inc.)

P20 Carbon Nanotube Field-Effect Transistor Performance in the Scope of the 2026 ITRS Recommendations
(A. Pacheco-Sanchez[1], D. Loroch[1], S. Mothes[1,2], M. Schröter[1,3], M. Claus[1,2] ([1]Department of Electrical and Computer Engineering, Technische Universität Dresden; [2] Center for Advancing Electronics Dresden, Technische Universität Dresden; [3] Department of Electronics and Communication Engineering, University of California at San Diego)